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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,990,063 B1

Confirmation No. 9726

Issued: January 24, 2006

Name of Patentee: Lenoski et al.

Patent Title: DISTRIBUTING FAULT INDICATIONS AND MAINTAINING AND USING A DATA STRUCTURE INDICATING FAULTS TO ROUTE TRAFFIC IN A PACKET SWITCHING SYSTEM

Certificate
MAR 30 2006
of Correction

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on March 21, 2006.

Kirk D. Williams, Esq. 3/21/2006

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PATENT OFFICE MISTAKE (37 C.F.R. § 1.322)

Attn: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

It is requested that a Certificate of Correction be issued to correct Office mistakes found the above-identified patent. Attached hereto is a Certificate of Correction which indicates the requested correction. For your convenience, also attached are copies of selected pages (a) from the issued patent with errors highlighted, and (b) from Amendment A filed January 6, 2004, with the correct text/instructions.

MAR 31 2006

In re US Patent No. 6,990,063 B1

It is believed that there is no charge for this request because applicant or applicants were not responsible for such error, as will be apparent upon a comparison of the issued patent with the application as filed or amended. However, the Assistant Commissioner is hereby authorized to charge any fee that may be required to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: March 21, 2006

By _____ 3/21/2006
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,990,063 B1

DATED : January 24, 2006

INVENTOR(S) : Lenoski et al.

It is certified that error(s) appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 5, line 25, replace "signals. 201" with -- signals 201 --

MAILING ADDRESS OF SENDER:
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PATENT NO. 6,990,063
No. of additional copies

⇨ NONE (0)

MAR 31 2006

From Amendment A filed 1-6-2004

Please replace the paragraph beginning on page 8, line 4 with the following amended paragraph:

Line card 270 illustrated in FIG. 2C includes control logic 271 to control operations of the ~~input/output interface~~ line card 270. Control logic 271 is connected to other components of line card 270 via one or more internal communications mechanisms 279 (shown as a bus for illustrative purposes). In one embodiment, control logic 271 includes memory for storing instructions and data. Line card 270 also includes optional additional memory 272 and storage devices 273. External interface receiver 274 receives external signals 201 (FIG. 2), separates the signals into channels using ~~demultiplexor~~ demultiplexer 275 into multiple streams of packets which are temporarily stored in incoming packet buffer 276. At the appropriate time, a packet is sent to switch interface 290 via transmitter to switch interface 277. Packets are received from switch interface 290 at the receiver from switch interface 287 and placed in the outgoing packet buffer 286. ~~Multiplexor~~ Multiplexer 285 extracts the packets and creates a multiplexed signal which is transmitted via external interface transmitter 284. In one embodiment, control logic 271, referencing a data structure within control logic 271 or memory 272, stores fault indications. Line card 270 may receive, generate, process and react to fault indications as described hereinafter. In certain embodiments, fault conditions may be hidden from a line card by other components which react to the fault indications.

purposes). External interface receiver **250** receives external signals, converts these signals using demultiplexer **251** into multiple streams of packets which are temporarily stored in incoming packet buffer **252**. At the appropriate time, a packet is sent to the appropriate switch element SE-1 & SE-3 **162** via transmitter to switch elements **253**. Packets are received from switch elements SE-1 & SE-3 **162** at the receiver from switch elements **263** and placed in the outgoing packet buffer **262**. Multiplexer **261** extracts the packets and creates a multiplexed signal that is transmitted via external interface transmitter **260**. Additionally, control logic **241** receives, generates, processes and reacts to fault indications as described hereinafter.

FIG. 2C illustrates one embodiment of a line card **270** and a switch interface **290**, which could correspond to line card **159** and input/output interfaces **169** illustrated in FIG. 2C.

Line card **270** illustrated in FIG. 2C includes control logic **271** to control operations of the line card **270**. Control logic **271** is connected to other components of line card **270** via one or more internal communications mechanisms **279** (shown as a bus for illustrative purposes). In one embodiment, control logic **271** includes memory for storing instructions and data. Line card **270** also includes optional additional memory **272** and storage devices **273**. External interface receiver **274** receives external signals. **201** (FIG. 2), separates the signals into channels using demultiplexer **275** into multiple streams of packets which are temporarily stored in incoming packet buffer **276**. At the appropriate time, a packet is sent to switch interface **290** via transmitter to switch interface **277**. Packets are received from switch interface **290** at the receiver from switch interface **287** and placed in the outgoing packet buffer **286**. Multiplexer **285** extracts the packets and creates a multiplexed signal which is transmitted via external interface transmitter **284**. In one embodiment, control logic **271**, referencing a data structure within control logic **271** or memory **272**, stores fault indications. Line card **270** may receive, generate, process and react to fault indications as described hereinafter. In certain embodiments, fault conditions may be hidden from a line card by other components which react to the fault indications.

Signals 201

The embodiment of input/output interface **290** illustrated in FIG. 2C includes control logic **291** implementing functionality in accordance with certain embodiments of the invention. Control logic **291** is connected to other components of switch interface **290** via one or more internal communications mechanisms **289** (shown as a bus for illustrative purposes). In one embodiment, control logic **291** includes memory for storing instructions and data. Switch interface **290** also includes optional additional memory **292** and storage devices **293**. Line card receiver **294** receives packets from line card **270** temporarily stores the packets in incoming packet buffer **295**. At the appropriate time, a packet is sent to an appropriate switch element SE-1 & SE-3 **162** via transmitter to switch elements **296**. Packets are received from switch elements SE-1 & SE-3 **162** at the receiver from switch elements **299** and placed in the outgoing packet buffer **298**. Line card interface transmitter **297** then forwards these packets to line card **270**. In one embodiment, control logic **291**, referencing a data structure within control logic **291** or memory **292**, stores fault indications which could be received from a line card, packet switch, or internally generated. Input/output interface **290** receives, generates, processes and reacts to fault indications as described hereinafter.

FIGS. 3A–C illustrate exemplary embodiments of switching elements and/or their components. FIG. 3A is a block diagram of one embodiment of a first stage switching element, SE-1 **300**. FIG. 3B is a block diagram of one embodiment of a second stage switching element SE-2 **330**. FIG. 3C is a block diagram of one embodiment of a third stage switching element SE-3 **360**. As would be understood by one skilled in the art, the invention is not limited to these or any other embodiment described herein.

FIG. 3A illustrates an embodiment of SE-1 **300** comprising control logic and/or processor **311** (hereinafter "control logic"), memory **312**, storage devices **310**, I/O interfaces **305**, output queues **320**, SE-2 interfaces **325**, and one or more internal communications mechanisms **319** (shown as a bus for illustrative purposes). In certain embodiments, control logic **311** comprises custom control circuitry for controlling the operation of SE-1 **300** and no storage device **310** is used. Memory **312** is one type of computer-readable medium, and typically comprises random access memory (RAM), read only memory (ROM), integrated circuits, and/or other memory components. Memory **312** typically stores computer-executable instructions to be executed by control logic **311** and/or data which is manipulated by control logic **311** for implementing functionality in accordance with certain embodiments of the invention. Storage devices **310** are another type of computer-readable medium, and may comprise, for example, disk drives, diskettes, networked services, tape drives, and other storage devices. Storage devices **310** typically store computer-executable instructions to be executed by control logic **311** and/or data which is manipulated by control logic **311** for implementing functionality disclosed herein.

SE-1 **300** generates, consumes, processes and reacts to fault indications as further described in detail hereinafter. Briefly first, each SE-1 **300** receives packets **301** and exchanges control messages **302** over one or more links with one or more input interfaces (not shown) such as input/output interface **290** (FIG. 2C) via I/O interfaces **305**. Additionally, each SE-1 **300** sends packets **328** and exchanges control messages **329** over one or more links with one or more SE-2 elements (not shown) such as SE-2 **330** (FIG. 3B) via SE-2 interfaces **325**. Control logic **311** detects faults, generates control packets containing indications of the detected faults, and updates its fault data structure stored in memory **312**. SE-1 **300** may distribute fault indications to other packet switching components by sending control packets to other components as well as including fault indications in reserved fields of other control messages (e.g., acknowledgment or clear-to-send control messages) being sent. Outgoing packets and control messages are placed in output queues **320**. In one embodiment, there is an output queue **320** for each destination, or for each class of service for each destination.

FIG. 3B illustrates an embodiment of SE-2 **330** comprising control logic and/or processor **341** (hereinafter "control logic"), memory **342**, storage devices **340**, SE-1 interfaces **335**, output queues **350**, SE-3 interfaces **355**, and one or more internal communications mechanisms **349** (shown as a bus for illustrative purposes). In certain embodiments, control logic **341** comprises custom control circuitry for controlling the operation of SE-2 **330** and no storage device **340** is used. Memory **342** is one type of computer-readable medium, and typically comprises random access memory (RAM), read only memory (ROM), integrated circuits, and/or other memory components. Memory **342** typically stores computer-executable instructions to be executed by control logic **341** and/or data which is manipulated by control logic **341** for implementing functionality described herein. Storage devices **340** are another type of computer-readable